UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,803	01/13/2004	Chao-Cheng Lee	REAP0003USA	1802

27765 7590 05/12/2005

NORTH AMERICA INTERNATIONAL PATENT OFFICE (NAIPC)
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
NGUYEN, LINH V	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 05/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,803	LEE ET AL.	
	Examiner	Art Unit	
	Linh V. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-20* is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to application No. 10/707803 filed on 01/13/04. Claims 1 – 20 are pending on this application.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2 and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Gulati et al. Pub. No.: US 2003/0146786 A1.

Regarding claim 1, Fig. 6 of Gulati et al. discloses a circuit comprising: an operational amplifier (162) comprising a positive input end (positive input terminal of 162), a negative input end (Negative Input terminal of 162), and an output end (output terminal of 162); a first input impedance (C1+) coupled between the negative input end and a first input signal (Vin+); a second input impedance (C1-) coupled between the negative input end and a second input signal Vin-); and a first output impedance (Cf+)

coupled between the negative input end and the output end, wherein resistances of the first and second input impedances are controlled by a first and a second control signals respectively (see controlling switches CL1, CL2 for controlling the resistance value of the first C1+ and second C- input impedance).

Regarding claim 2, wherein resistances of the first and second input impedances are close to each other (both input impedance had the same value C1 therefore the resistance value of both inputs is the same).

Regarding claim 6, wherein the first input impedance (C1+) is a switched capacitor circuit (CL1, CL2), the switched capacitor circuit comprises: a capacitor (C1+) coupled between a first node and a ground end (C1+ coupled between the ground end via S4 and left node of C1+); a first switch (S1) with one end coupled to the first node (left node of C1+) and another end (V1+) used as an end of the switched capacitor circuit; and a second switched (S2) with one end coupled to the first node (left node of C1+) and another end (Ground) used as another end of the switched capacitor circuit, wherein the first switch and the second switch (S1, S2) are turned on alternately by the first control signal (CL1, CL2).

3. Claims 7, and 8 - 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Kuttner U.S. patent No. 6,707,405.

Regarding claim 7, Fig. 2 of Kuttner disclose a circuit comprising: a differential amplifier (OP1) comprising a positive input end (+), a negative input end (-), a positive output end (positive output of OP1), and a negative output end (NE); a first input impedance (R6) coupled between the negative input end (NE) and a first input signal

(ME1); a second input impedance (R8) coupled between the positive input end (PE) and the first input signal (ME1); a third input impedance (R7) coupled between the negative input end (NE) and a second input signal (ME2), the third input impedance being substantially equivalent to the second input impedance (Col. 5 lines 46 – 50); a fourth input impedance (R9) coupled between the positive input end (PE) and the second input signal (ME2), the fourth input impedance being substantially equivalent to the first input impedance (Col. 5 lines 46 – 50); wherein resistances of the first and second input impedances are controlled by a first and a second control signals respectively (S6, S8).

Regarding claim 8, wherein resistances of the first and second input impedances are close to each other (Col. 5 lines 46 – 50).

Regarding claim 9, wherein the circuit has put impedance characteristic (Col. 2 lines 10 – 11).

Regarding claim 10, Fig. 2 of Kuttner further comprising: a first output impedance (R4) coupled between the negative input end (NE) and the positive output end (VPA); and a second output impedance (R5) coupled between the positive input end (PE) and the negative output end (VNA).

Regarding claim 11, wherein the first and the second output impedances are a resistive-impedance (R4, R5), the circuit has a high voltage attenuation characteristic (hence on Col. 2 lines 10 – 11 Kuttner discloses a high input impedance circuit therefore R4 and R5 must have high voltage attenuation characteristic).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gulati et al. as applied to claim 2 above.

Regarding claim 3, Gulati et al. as applied to claim 2 above do not explicitly disclose the circuit has high input impedance circuit. However, the input impedance characteristic circuit is depend upon the resistance value of the input impedance, and the input impedance C1+, and C- of Gulati et al must have either high or low resistance value. Therefore, it would have been obvious to one have ordinary skill in the art at the time the invention was made to have a high input impedance characteristic according to the design of interests, because the input impedance C1+, and C- of Gulati et al. must has either high or low resistance value.

Regarding claim 5 Gulati et al. as applied to claim 2 above further disclose wherein the first output impedance is a capacitive-impedance (Cf+), but does not disclose the circuit has a large time constant characteristic. However, larger or small the time constant of the circuit is depending upon the capacitance value of the capacitive-impedance. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have a large time constant according to the

design of interests, because the capacitive-impedance CF+ of Gulati et al. must has either high or low time constant value.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gulati et al. as applied to claim 2 above, in view of Sobel U.S. Patent 6,833,759

Gulati et al. as applied to claim 2 above, does not disclose wherein the first output impedance is a resistive-impedance, the circuit has a high voltage attenuation characteristic.

Fig. 4 of Sobel discloses a differential amplifier circuit having the first output impedance is a resistive-impedance (401) with high voltage attenuation characteristic (406a1- 406an).

Gulati et al. and Sobel are common subject matter for controlling impedance of differential amplifier circuit. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the resistive output impedance taught by Sobel incorporated into the output impedance of Gulati et al. for the purpose of providing passive attenuation therefore the total complexity of the feedback of the amplifier can be reduced (Sobel, Col. 4 lines 1 – 8).

7. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuttner, in view of Gulati et al. as applied to claim 5 above.

Regarding claim 12, Kuttner as applied to claim 10 above, does not discloses wherein at least one the first (and the second output impedance (R4, R5) is a capacitive-impedance, the circuit has a large time constant characteristic.

Gulati et al. as applied to claim 2 above further disclose wherein the first output impedance is a capacitive-impedance (Cf+) with large time constant.

Kuttner and Gulati et al. are common subject matter for differential amplifier. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modified the resistive output impedance of Kuttner with the capacitive-impedance output taught by Gulati et al. for the purpose of providing the capacitive output impedance according to design of interest.

Regarding claim 13, Kuttner as applied to claim 7 above, does not discloses the first input impedance of his is a switched capacitor circuit, and the switched capacitor circuit comprises: a capacitor coupled between a first end ; node and a ground a first switch with one end coupled to the first node and another end used as an end of the switched capacitor circuit; and a second switch with one end coupled to the first node and another end used as another end of the switched capacitor circuit, wherein the first switch and the second switch are turned on alternately by the first control signal.

Gulati et al. as applied to claim 6 above discloses the first input impedance (C1+) is a switched capacitor circuit (CL1, CL2), the switched capacitor circuit comprises: a capacitor (C1+) coupled between a first node and a ground end (C1+ coupled between the ground end via S4 and left node of C1+); a first switch (S1) with one end coupled to the first node (left node of C1+) and another end (V1+) used as an end of the switched capacitor circuit; and a second switched (S2) with one end coupled to the first node (left node of C1+) and another end (Ground) used as another end of the switched capacitor

circuit, wherein the first switch and the second switch (S1, S2) are turned on alternately by the first control signal (CL1, CL2).

Kuttner and Gulati et al. are common subject matter for input impedance of differential amplifier circuit. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the switched resistive input impedance of Kuttner with the switched capacitor impedance taught by Gulati et al. for the purpose of providing switched capacitor circuit where it is desirable to minimizing circuit offset and low frequency noise (Gulati et al.'s last 3 lines of paragraph 0008).

Allowable Subject Matter

8. Claims 14 – 20 are allowed.

9. The following is an examiner's statement of reasons for allowance:

With respect to claims 14 and 19, in addition to other elements in each respective claim, the prior are doest not teach or suggest a differential amplifier a first output impedance coupled between the negative input end and the positive output end; a second output impedance coupled between the negative input end and the negative output end; a third output impedance coupled between the positive input end and the positive output end; and a fourth output impedance coupled between the positive input end and the negative output end, wherein resistances of the impedances are first and second output controlled by a first and a second control signals respectively..

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Prior Art

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Contact Information

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Michael Tokar can be reached at (571) 272-1812. The fax phone numbers for the organization where this application or proceeding is assigned are (703-872-9306) for regular communications and (703-872-9306) for After Final communications.

4/26/05

Linh Van Nguyen

Art Unit 2819